

Docket No.: P2001,0368

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By: 

Date: January 2, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No. : 10/724,903
Applicant : Grit Schwalbe et al.
Filed : December 1, 2003
Art Unit : to be assigned
Examiner : to be assigned

Docket No. : P2001,0368
Customer No. : 24131

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner for Patents

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 5,168,334 (Mitchell et al.), dated December 1, 1992;

United States Patent No. 5,768,192 (Eitan), dated June 16, 1998;

United States Patent No. 5,815,433 (Takeuchi), dated September 29, 1998;

United States Patent No. 5,915,203 (Sengupta et al.), dated June 22, 1999;

United States Patent No. 5,963,465 (Eitan), dated October 5, 1999;

United States Patent No. 5,966,603 (Eitan), dated October 12, 1999;

United States Patent No. 6,133,095 (Eitan et al.), dated October 17, 2000;

Takhyun Yoon et al.: "A New Process Integration – P³ (Pre Poly Plug) – for Giga Bit DRAM Era", *Symposium on VLSI Technical Digest, August 1999, 2 pgs.*;

Jong-Wan Jung et al.: "A fully working 0.14µm DRAM technology with polymetal (W/WNx/Poly-Si) gate", *IEEE, 2000, 4 pgs.*;

International Search Report dated February 21, 2003;

International Preliminary Examination Report dated August 19, 2003.

As per the Notice in 1273 OG 55 (August 5, 2003) no copies of any above-mentioned U.S. patents and U.S. patent application publications are submitted for any application filed after June 30, 2003.

Respectfully submitted,



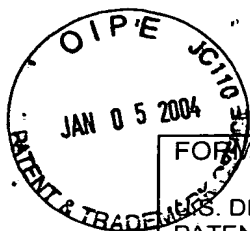
For Applicants

Date: January 2, 2004

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FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.:

P2001,0368

Applic. No.

10/724,903

Applicant

Grit Schwalbe et al.

Filing Date

December 1, 2003

Group Art Unit

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | PATENT NO. | DATE | PATENTEE | CLASS | SUB CLASS | FILING DATE |
|----------------------|---|------------|----------|-----------------|-------|--------------|----------------|
| | A | 5,168,334 | 12/01/92 | Mitchell et al. | | | |
| | B | 5,768,192 | 06/16/98 | Eitan | | | |
| | C | 5,815,433 | 09/29/98 | Takeuchi | | | |
| | D | 5,915,203 | 06/22/99 | Sengupta et al. | | | |
| | E | 5,963,465 | 10/05/99 | Eitan | | | |
| | F | 5,966,603 | 10/12/99 | Eitan | | | |
| | G | 6,133,095 | 10/17/00 | Eitan et al. | | | |
| | H | | | | | | |
| | I | | | | | | |

FOREIGN PATENT DOCUMENT

| | | DOCUMENT NO. | DATE | COUNTRY | CLASS | SUB CLASS | TRANSL. YES NO |
|--|---|--------------|------|---------|-------|--------------|---------------------|
| | J | | | | | | |
| | K | | | | | | |
| | L | | | | | | |
| | M | | | | | | |
| | N | | | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

| | | |
|--|---|--|
| | O | Takhyun Yoon et al.: "A New Process Integration – P ³ (Pre Poly Plug) – for Giga Bit DRAM Era", <i>Symposium on VLSI Technical Digest, August 1999</i> , 2 pgs. |
| | P | Jong-Wan Jung et al.: "A fully working 0.14µm DRAM technology with polymetal (W/WNx/Poly-Si) gate", <i>IEEE, 2000</i> , 4 pgs. |

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.